



INFORMATION DISCLOSURE STATEMENT

Applicant : Songjie Xu
App. No. : 09/754,406
Filed : January 2, 2001
For : METHODOLOGY AND APPLICATIONS
OF TIMING-DRIVEN LOGIC
RESYNTHESIS FOR VLSI CIRCUITS
Examiner : Mary C. Hogan
Group Art Unit : 2123

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Dear Sir:

Enclosed is form PTO-1449 listing two (2) references that are also enclosed.

This Information Disclosure Statement is being filed under 37 C.F.R. § 1.97(c)(2) before the mailing date of a final action and before the mailing of a Notice of Allowance. This Statement is accompanied by the fees set forth in 37 C.F.R. § 1.17(p). The Commissioner is hereby authorized to charge any additional fees which may be required or to credit any overpayment to Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: November 24, 2004By: Raimond J. Salenieks

Raimond J. Salenieks
Registration No. 37,924
Agent of Record
Customer No. 20,995
(619) 235-8550

FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
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09/754,406INFORMATION DISCLOSURE STATEMENT
BY APPLICANT

(USE SEVERAL SHEETS IF NECESSARY)

APPLICANT
Songjie XuFILING DATE
January 2, 2001GROUP
2123

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

EXAMINER
INITIAL

OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

	1	Songjie Xu, <i>Synthesis for High-Density and High-Performance FPGAs</i> , dissertation submitted to University of California, Los Angeles, August 31, 2000
	2	Singh, Kanwar Jit, Ph.D., <i>Performance Optimization of Digital Circuits</i> , dissertation submitted to University of California, Berkeley, 1992

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